IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Hutton

Attorney Docket No.: ALTRP061/A637

Application No.: 09/783,246

Examiner: Not yet assigned

Filed: February 13, 2001

Group: 2644

Title: METHOD FOR ADAPTIVE CRITICAL PATH DELAY ESTIMATION DURING TIMING-DRIVEN PLACEMENT FOR HIERARCHICAL PROGRAMMABLE LOGIC DEVICES

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on May 24, 2004 in an envelope addressed to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

Signed: _____
Mia Mitchell-Haynes

INFORMATION DISCLOSURE STATEMENT
37 CFR §§1.56 AND 1.97(b)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

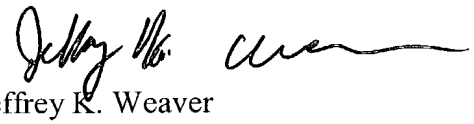
The references listed in the attached PTO Form 1449, copies of which are attached, may be material to examination of the above-identified patent application. Applicants submit these references in compliance with their duty of disclosure pursuant to 37 CFR §§1.56 and 1.97. The Examiner is requested to make these references of official record in this application.

This Information Disclosure Statement is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that these references indeed constitute prior art.

This Information Disclosure Statement is: (i) filed within three (3) months of the filing date of the above-referenced application, (ii) believed to be filed before the mailing date of a first Office Action on the merits, or (iii) believed to be filed before the mailing of a first Office Action after the filing of a Request for Continued Examination under §1.114. Accordingly, it is believed that no fees are due in connection with the filing of this Information Disclosure

Statement. However, if it is determined that any fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 500388 (Order No. ALTRP061).

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP



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/Form 1449 (Modified)	Atty Docket No.	Application No.:
	ALTRP061	09/783,246
Information Disclosure Statement By Applicant	Applicant: Hutton	
	Filing Date	Group
(Use Several Sheets if Necessary)	2/13/01	2644

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A1	5,550,782	8/27/96	Cliff et al.			5/18/94
	A2	5,689,195	11/18/97	Cliff et al.			5/17/95
	A3	6,215,326	4/10/01	Jefferson et al.			3/10/99
	A4	5,659,484	8/19/97	Bennett et al.			

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	B1	Hutton et al., "Timing-Driven Placement for Hierarchical Programmable Logic Devices". Talk describing aspects of the invention. Monterey, California –February 11, 2001 (paper attached).
	B2	V. Betz, Architecture and CAD for Speed and Area Optimization of FPGA's", Ph.D. Dissertation, University of Toronto, 1998.
	B3	Jason Cong et al., "Large Scale Circuit Partitioning with Loose/Stable Net Removal and Signal Flow Based Clustering", Proc. IEEE Int'l Conference on Computer-Aided Design, pp. 441-446, November 1997.
	B4	W.E. Donath et al., "Timing Driven Placement Using Complete Path Delays", in Proc. 27th ACM/IEEE Design Automation Conference, pp.84-89, 1990.
	B5	Carl Ebeling et al., "Placement and Routing Tools for theTriptych FPGA", IEEE Trans. On VLSI, Vol. 3, No. 4, pp. 473-481, December 1995.
	B6	Jon Frankle, "Iterative and Adaptive Slack Allocation for Performance-Driven Layout and FPGE Routing", in Proc. 29th ACM/IEEE Design Automation Conference, pp 536-542, 1992.

Examiner	Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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Information Disclosure Statement By Applicant	ALTRP061 Applicant: Hutton	09/783,246
(Use Several Sheets if Necessary)	Filing Date 2/13/01	Group 2644

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	B7	P. Leventis, "Placement algorithms and routing architecture for long-line based FPGA's", Bachelor thesis, University of Toronto 1999.
	B8	Alexander Marquardt et al., "Timing-Driven Placement for FPGA's", in Proc. ACM/SIGDA FPGA Conference, FPGA00, pp. 203-213, 2000.
	B9	Sudip K. Nag and Rob A. Rutenbar, "Performance-Driven Simultaneous Placement and Routing for FPGA's". IEEE Trans. On CAD for Integrated Circuits and Systems, Vol. 17, No. 6, pp. 499-518, June 1998.
	B10	Shih-Lian Ou and Massoud Pedram, "Timing-Driven Placement Based on Partitioning with Dynamic Cut-net Control", in Proc. 37th ACM/IEEE Design Automation Conference, pp. 472-476, 2000.
	B11	Laura A. Sanchis, "Multiple-way network partitioning", IEEE Trans. On Computers, Vol. 38, No. 1, January 1989.
	B12	Prashant Sawkar and Donald Thomas, "Multi-Way Partitioning for Minimum Delay for Look-Up Table Based FPGAs". In Proc. 32nd ACM/IEEE Design Automation Conference, pp. 201-205, 1995.
	B13	S.A. Senouci et al., "Timing-Driven Floorplanning on Programmable Hierarchical Targets", in Proc. ACM/SIGDA FPGA Conference, FPGA98, pp. 85-92, 1998.
	B14	S. Sutanthavibul and E. Shragowitz, "Dynamic Prediction of Critical Paths and Nets for Constructive Timing-Driven Placement", in Proc. 28th ACM/IEEE Design Automation Conference, pp. 632-635, 1991.
	B15	W. Swartz and C. Sechen, "Timing-Driven Placement for Large Standard Cell Circuits", in Proc. 32nd ACM/IEEE Design Automation Conference, pp. 211-215, 1995.

Examiner	Date Considered

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